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Performance Analysis of Nanoelectromechanical Relay-Based Field-Programmable Gate Arrays

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ABSTRACT The energy consumption of field-programmable gate arrays (FPGA) is dominated by leakage currents and dynamic energy associated with programmable interconnect. An FPGA built entirely from nano-electromechanical (NEM) relays can effectively eliminate leakage energy losses, reduce the interconnect dynamic energy, operate at temperatures >225 °C and tolerate radiation doses in excess of 100 Mrad, while hybrid FPGAs comprising both complementary metal-oxide-semiconductor (CMOS) transistors and NEM relays (NEM-CMOS) have the potential to realize improvements in performance *and* energy efficiency. Large-scale integration of NEM relays, however, poses a significant engineering challenge due to the presence of moving parts. We discuss the design of FPGAs utilizing NEM relays based on a heterogeneous 3-D integration scheme, and carry out a scaling study to quantify key metrics related to performance and energy efficiency in both NEM-only and NEM-CMOS FPGAs. We show how the integration scheme has a profound effect on these metrics by changing the length of global wires. The scaling regime beyond which net performance and energy benefits is seen in NEM-CMOS over a baseline 90 nm CMOS technology is defined by an effective relay beam length of 0.5 μm, on-resistance of 200 kΩ, and a via pitch of 0.4 μm, all achievable with existing process technology. For ultra-low energy applications that are not performance critical, NEM-only FPGAs can provide close to 15× improvement in energy efficiency.

INDEX TERMS Nanoelectromechanical, microelectromechanical, relay, non-volatile, 3-terminal, 4-terminal, nano switch, MEMS, NEMS, FPGA, energy efficiency, high-temperature, radiation-hard, integration, back-end-of-line, CMOS.

I. INTRODUCTION

Field programmable gate arrays (FPGA) are increasingly used in many high-value and safety-critical markets, as they significantly lower development and manufacturing costs and improve design productivity. Improving energy efficiency, especially at elevated temperatures and high levels of radiation common in many industrial, aerospace and security applications, would greatly widen their deployment space. Nanoelectromechanical (NEM) relays are promising candidates to be used in lieu of transistors in such harsh environments as they have zero leakage in the off-state, a steep subthreshold slope [1], can potentially operate at temperatures over 225 °C (with near zero leakage unlike alternative high-temperature technologies such as SiC MOSFETs [2]), and tolerate radiation doses in excess of 100 Mrad [3]. Despite the fact that NEM relays contain suspended mechanical beams, such structures are typically not affected by shock or vibrations due to their extremely small mass [4].

While managing the contact reliability has been a major challenge, recent work has shown that using monocrystalline silicon relays with forms of carbon to act as a protective layer has potential to substantially improve the contact reliability [5], [6], opening up the possibility of realising reliable NEM relay-based FPGAs. However, NEM relay-based circuits pose unique integration challenges as they have moving parts, making it very challenging to fabricate a metal interconnect stack on top of devices as is done in complementary metal-oxide-semiconductor (CMOS) integrated circuits (IC). Instead, large-scale integration can be achieved by forming relays on top of metal interconnect layers, as shown in Fig. 1. Such integration of NEM relay circuits can be achieved by approaches that can be collectively

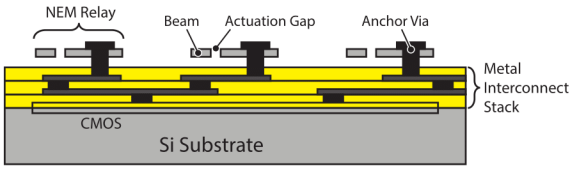


FIGURE 1. Cross-section of a NEM-CMOS IC showing NEM relays and vias connecting them to the top metal layer on a multi-layer interconnect stack. CMOS circuits are also shown, connected to the same interconnect stack.

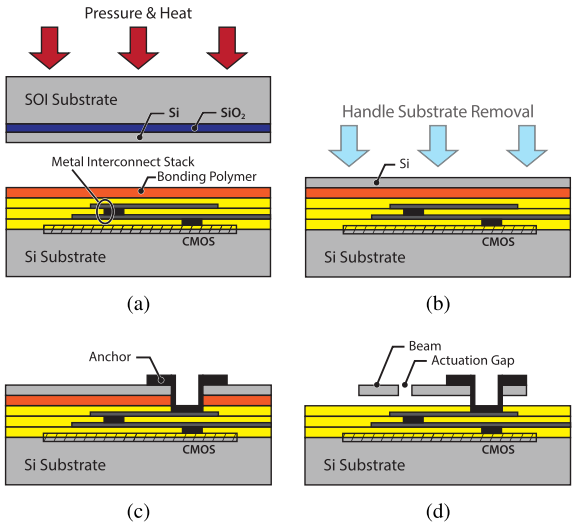


FIGURE 2. NEM relay integration based on via-last, heterogeneous 3-D integration: (a) bonding of an SOI wafer to a back-end-of-line (BEOL) wafer using a thin bonding polymer layer; (b) removal of SOI handle substrate and oxide; (c) etching of via holes and deposition of metal anchors for electrical connection of NEM relays to interconnect layers; and (d) structuring of NEM relays and release etching by sacrificial removal of polymer layer [12].

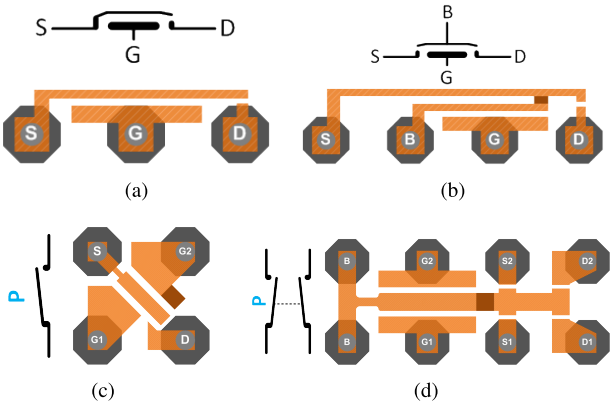


FIGURE 3. Abstract representations of layout with vias for anchoring and electrical contact to interconnect wafer, and accompanying symbol: (a) 3-T relay; (b) 4-T relay; (c) dual-gate NV relay; and (d) dual-gate 4-T NV relay. S, G, D, and B refer to source, gate, drain and body respectively by analogy to transistors.

classified as monolithic integration [7]–[11], or heteogeneous integration [12], [13].

Both monolithic integration and heterogeneous 3-D integration using via-last approaches offer the possibility to realize NEM device dimensions and via pitches that are essentially only limited by the capability of the available lithography processes, which can be in the sub-μm range. However, heterogeneous 3-D integration approaches offer flexible material choices, such as mono-crystalline silicon in combination with carbon-based contact materials for the NEM relays – especially important for realizing highly reliable switching. By contrast, in monolithic integration, NEM relay material choices are restricted to materials that can be deposited on top of the metal interconnect stack at comparatively low temperatures, typically $< 400\,^{\circ}\mathrm{C}$.

Despite the limitations of large footprint and high mechanical delay of NEM relays, Chen et al. identified an opportunity to *reduce* energy and latency in FPGAs, by using the relays as programmable switches in the interconnection network in combination with CMOS circuits [14]. They subsequently presented a simulation study to quantify performance improvements possible within a monolithic integration scheme [15]. By contrast, in this work, we carry out a simulation study of the performance of NEM-relay-based FPGAs based on a via-last heterogeneous 3-D integration scheme. We consider two separate architectures, *NEM-only* comprising NEM relays exclusively, targeting harsh-environment applications, and *NEM-CMOS* employing NEM relays in the interconnect switch matrix, targeting performance and energy improvements over CMOS-only implementations. The study identifies two separate scaling parameters, related to relay size and integration via pitch, each of which independently define different axes in the design space.

The contributions of this paper are firstly in carrying out a comprehensive study based on via-last heterogeneous integration, which appears to hold out more promise to achieve reliable NEM-relay-based systems than monolithic integration. Secondly, it quantifies performance with on-resistance and scaled dimensions of integration pitch and relay footprint for NEM-only and NEM-CMOS systems, providing insight into how such systems can be designed under performance and energy constraints.

II. TECHNOLOGY PLATFORM AND MODELING

For investigating performance of both NEM-only and NEM-CMOS FPGAs in this work, we assume the NEM relays are placed on top of a metal interconnect stack, as shown in Fig. 1. Additionally, in the NEM-CMOS FPGA implementation, CMOS circuits are present underneath the metal interconnect stack, which is shared by the NEM relays and CMOS. This configuration can be realized, for example, by a "via-last" heterogeneous 3-D integration process as outlined in Fig. 2, in which the silicon device layer of a silicon-on-insulator (SOI) wafer is transferred to a wafer containing a metal interconnect stack (and CMOS circuits where required) from a standard CMOS foundry

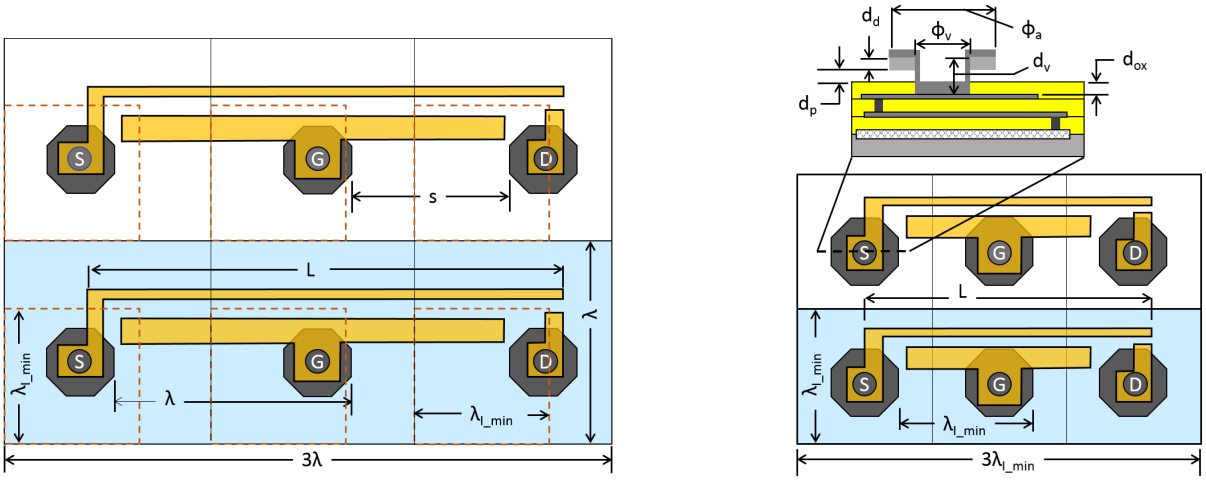


FIGURE 4. Representative, architecture-agnostic layout for 3-T relay where the minimum integration pitch λ_{I_min} is the same size in both cases, but the relay size is different: (a) relay footprint dictated by relay size, i.e. $\lambda > \lambda_{I\_min}$; and (b) relay footprint is dictated by via pitch i.e. $\lambda = \lambda_{I\_min}$.

offering [13], [16]. Consequently, vias[1] and NEM relays are formed.

In our scaling study we model 3-terminal (3-T), 4-terminal (4-T) and non-volatile (NV) NEM relays (see Fig. 3) with different footprints. 3-T relays have a simpler fabrication process and smaller footprint than 4-T relays that decouple control and signal voltages, but require more devices for a given function. The functionality of the 3-T dual-gate NV relay (Fig. 3(c)) is that a programming voltage V_{G1} causes the beam S to make contact with the drain electrode D, and stays in contact when V_{G1} is removed. A voltage V_{G2} causes the beam to move out of contact. The 4-T NV relay decouples the programming and data electrodes. All of the schematics in Fig. 3 are architecture-agnostic, and Section II-B describes how actual implementations are mapped to these primitives in our analysis. The 3-T, 4-T and NV relay footprints collectively form the relay technology scaling "node" while the via densities represent the scaling node for integration. Thus there are two independent scaling parameters, and the following sections describe the modeling basis for each.

A. SCALING OF THE INTEGRATION NODE

Scaling of the via pitch in the configuration shown in Fig. 1 follows a completely different pathway to, and is independent of, relay scaling. All parameters referred to below are defined in Fig. 4. The achievable minimum via pitch, λ_{I_min}, is determined by the size of the anchor head, whose diameter is ϕ_a, and the space between anchors, S, in the relay structure. Here ϕ_a is the sum of the via-hole diameter ϕ_v and the overhang around the via. Based on considerations of resolution and alignment accuracy in existing lithography technology [17], [18], the minimum anchor via diameter ϕ_{a_min} is approximated as $\frac{4}{3}\phi_v$. Thus,

$$\lambda_{I\_min} = S_{min} + \phi_{a\_min} = S_{min} + \frac{4}{3}\phi_{v\_min}. \quad (1)$$

Here S_{min} is only limited by the lithography feature size, and, in theory, can be as small as the NEM relay actuation gap (tens of nm). However, it is important to keep the anchor-via-to-anchor-via and anchor-via-to-relay parasitic capacitances low. Having small parasitic capacitances is key to low energy operation in NEM relay-based circuits, as they have negligible leakage and the energy consumption is purely dynamic. Hence, we define a spacing design rule, that the minimum space between two anchors is $S_{min} = \phi_{a\_min}$, giving

$$\lambda_{I\_min} = \frac{8}{3}\phi_{v\_min}. \quad (2)$$

Scaling of the via diameter is limited by the maximum allowed via aspect ratio, $\kappa = \frac{d_v}{\phi_v}$, where d_v is the via depth. Thus, for a given aspect ratio, ϕ_{v_min} is determined by the minimum achievable via depth d_{v_min}. The via depth d_v is determined by the combined thicknesses of the NEM device layer d_d, the air-gap between the substrate surface and the NEM device layer d_p, and top oxide layer d_{ox}, giving

$$\phi_{v\_min} = \frac{d_{v\_min}}{\kappa_{max}} \quad (3)$$

for $d_v = d_d + d_p + d_{ox}$. Based on our experiments, the current physical limits for the layer thicknesses are of the order of 60 nm for the silicon device layer to prevent relay beams bending out of plane, 30 nm for the air-gap (defined by the thickness of the polymer bonding layer) and 30 nm for the top oxide layer. The highest achieved aspect ratio for advanced technology nodes is $\kappa = 10$ as demonstrated recently [19] for metal filling in trenches. For metal filling in vias, the range

[1] We interchangeably use the terms "via" and "anchoring via" in the text to always refer to the vias that connect relays to the top metal layer, not to vias connecting different layers in the interconnect stack.

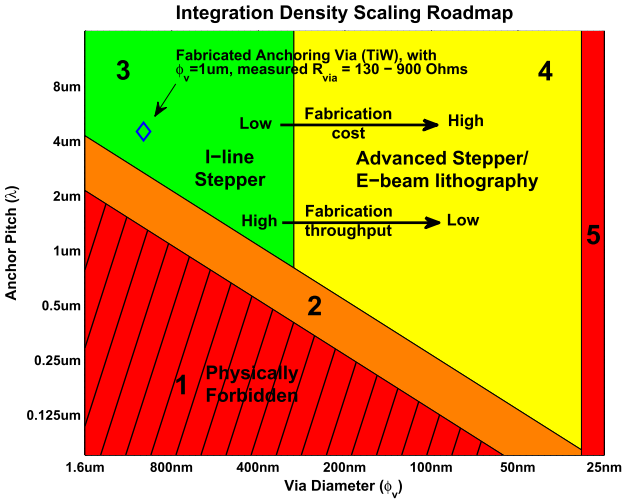


FIGURE 5. Scaling roadmap for proposed NEM relay integration scheme featuring five distinct regions. Via geometries are physically impossible in region 1, prohibited by design-rule constraints in 2, achievable through standard stepper [17] and deep UV or e-beam lithography [18] in 3 and 4 respectively, and unattainable in 5 with current capability ($\phi_v \approx 30$ nm). Measured R_{via} = 130 to 900 Ω at $\lambda = 4.5$ μm, $\phi_v = 1$ μm [see Fig. 7(c)].

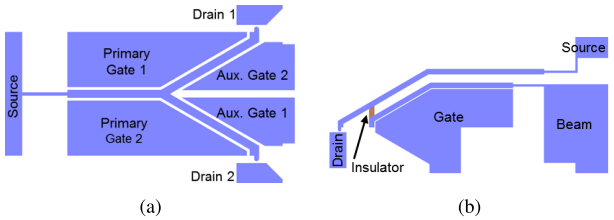


FIGURE 6. Relay architectures (a):3-T bi-directional relay with auxiliary gates; and (b):4-T relay with electrically isolating mechanical coupler.

for κ is much more conservative, and a range for high yield in processes that use sputtering is $0.5 \leqslant \kappa \leqslant 1$. For scaling we assume $\kappa_{max} = 4$.

With these values determining the physical limits, equations (1), (2) and (3) are used to generate the scaling roadmap of Fig. 5, showing the scaling of via pitch λ with via diameter ϕ_v. Region 1 in Fig. 5 reflects the design space where $\lambda \leqslant \frac{4}{3}\phi_{a\_min}$, which is physically impossible (limiting case being $S_{min} = 0$ in (1)). Region 2 reflects the forbidden design space $\phi_{a\_min} \leqslant \lambda \leqslant \frac{8}{3}\phi_{v\_min}$ imposed by the design rule. By reducing d_v, ϕ_v can be scaled down. When d_v is scaled close to its physical limit (of around 120 nm when all three layers hit the limit imposed by yield considerations) and the aspect ratio is the most aggressive at $\kappa = 4$, $\phi_{v\_min} = 30$ nm. Region 5 represents the space where $\phi_v \leqslant 30$ nm, and is unattainable under current process capability. However, with continuing development on the bonding process and via metallization, this limit may shrink in the future. When ϕ_v is scaled below 300 nm, which is smaller than the resolution of i-Line steppers [17], more advanced lithography tools such as deep-UV steppers or e-beam lithography need to be used [18]. This typically translates to drastically increased cost and reduced fabrication throughput. Regions 3 and 4 show the transition between process technologies. Shown in this scaling map is the fabricated integration node using TiW metal filling with anchor pitch of 4.5 μm and via-hole diameter of 1 μm (see Section II-D, *Model Validation*). The measured resistance per via is between 130 and 900 Ω.

B. NEM RELAY MODELING AND SCALING

The relay architecture for 3-T and 4-T relays used in the study are shown in Fig. 6, and have hinges and angled beams [5]. Similar to the architectures used by Parsa *et al.* [20] and Grogg *et al.* [21], the hinges act as the stress concentration region. The stress, and hence the deformation, along the rest of the beam is therefore minimal. The gate-to-beam gap, d, which is constant along the straight and angled length of the beam is equal to the drain-to-beam gap. In the closed state of the relay, the angled beam architecture helps maintain a safe air gap (0.16*d for a fork angle of 30°) near the free end of the beam. Such a geometry is easy to fabricate, requiring a single lithography step for the relay definition. A combination of the stress concentration feature and the angled architecture makes the beam less susceptible to collapse on the gate, which is a failure mechanism for straight cantilever beams [22]. The insulating coupler in the 4-T relay could be realised with an etch step after patterning, followed by blanket deposition of the insulating material (such as Si_3N_4) and a planarization step.

The critical relay parameters for performance evaluation in NEM-CMOS systems are the gate capacitance C_{gs} and on-resistance R_{on} (as the 4-T relays used in the interconnection matrices remain switched during run-time), while V_{DD} and the mechanical delay T_{mec} (time taken for the beam to pull-in after actuation) are also relevant for NEM-only systems. The rail voltage V_{DD} is determined by the pull-in voltage V_{pi} (as the pull-out voltage $V_{po} < V_{pi}$), i.e. $V_{DD} > V_{po}$. The voltages and T_{mec} are predicated on the relay architecture and effective beam length L_{eff}, C_{gs} on L_{eff} and rest actuation air-gap G_0, while R_{on} is primarily a function of the contact materials and beam electrode (tip) geometry. The effective area of an integrated relay includes the NEM relay itself, as well as the area occupied by the anchoring vias. For an n-terminal relay, the area $A = n\lambda^2$, for via pitch λ. It should be noted that the via pitch (and thus the relay footprint) with our heterogeneous 3-D integration scheme is limited either by the minimum achievable pitch for the vias in the integration scheme λ_{I_min}, or by the minimum achievable relay size (i.e. L_{eff_min}). If $\lambda > \lambda_{I\_min}$ the relay size determines the density, else λ_{I_min} is the limiting factor. These two scenarios are illustrated in Fig. 4 for a 3-T relay.

In the simulation study, five generations of relays, i.e. relay "nodes", characterised by L_{eff} and rest actuation air-gap G_0, are considered. Finite-element models (FEM) of the designs at each scaled node have been simulated using Ansys to extract V_{pi}, spring constant, k_{eff}, T_{mec} and C_{gs}, and the 3-T relay characteristics are presented in Table 1. The electrostatic force is sufficient to achieve pull-in at the

TABLE 1. Design parameters of (volatile) 3-T relay nodes extracted from FEM simulations.

L_{eff}	g_0	a	k_{eff}	V_{pi}	V_{DD}	T_{mec}	F_{adh}	F_s	C_{gs}	Comment
74 µm	1 µm	2.0 µm	2.86 N m^{-1}	49.2 V	55 V	2.12µs	47 nN	1.91 µN	1.21 fF	Measured V_{pi}=42 V, V_{po}=34 V
4 µm	50 nm	0.4 µm	0.65 N m^{-1}	2.26 V	3.0 V	175 ns	10.62 nN	21.7 nN	285 aF	
2 µm	25 nm	0.2 µm	0.32 N m^{-1}	1.13 V	2.0 V	69 ns	4.72 nN	5.33 nN	141 aF	
1 µm	15 nm	0.15 µm	0.31 N m^{-1}	0.83 V	1.5 V	38 ns	2.65 nN	3.10 nN	89.8 aF	
0.5 µm	10 nm	0.1 µm	0.24 N m^{-1}	0.69 V	1.2 V	24 ns	1.18 nN	1.60 nN	46.4 aF	

corresponding supply voltage V_{DD} with a margin of at least 0.5 V. One of the main considerations in design of NEM relays is that the spring force is sufficient to overcome surface adhesion forces to pull out upon deactivation. The surface adhesion force F_{adh} is generally dominated by the van der Waals force, which can be estimated based on the Hamaker approximation $F_{adh} = -\frac{HA_c}{6\pi D^3}$, where H is the Hamaker constant [23], A_c is the real contact area and D the separation. A_c depends on the number of asperities in contact, which in turn depends on the fabrication processes and materials used, and other factors such as the gate over-drive that are hard to estimate. We adopt a single-asperity model proposed in a previous study [24] for relays with a contact surface area of 2 µm and less, with an asperity radius that scales from 3 to 1 nm, a separation $D = 0.165$ nm and an estimated Hamaker constant for nanocrystalline graphite [5] of 10^{-20} J. The adhesion force thus calculated is shown in Table 1, and is always less than the spring force, increasing confidence in the viability of the designs. The extracted values for k_{eff} and T_{mec} are similar to those resulting from constant-field scaling [25].

In our study we assume that V_{pi}, and C_{gs} for 4-T and NV relays are the same as for 3-T relays for a given technology node (denoted by L_{eff}). The underlying premise is that 4-T and NV relays can be fabricated with the same effective beam length, for an identical pull-in voltage, which is reasonable given the relay architectures (see also Section II-D, model validation). To date, reported NV relays include devices that utilise trapped charge on a floating gate to change the threshold [26], and surface forces [8], [27]. It should be noted that state elements can be constructed from volatile relays using conventional circuits that utilise regenerative feedback, in the event that NV relays are not available within the technology platform. In this case the FPGAs do not retain their state on power-off, but are still reprogrammable, high-temperature and radiation-hard.

C. PERFORMANCE, AREA AND ENERGY MODELING

Delay in NEM relay-based circuits can be divided into a mechanical component and an electrical component [28]. The mechanical latency is predicated on the mechanical technology node, while the electrical component is dependent on the relay parasitics - a function of the relay technology node - but also of the interconnect parasitics. Thus, the size of the relay impacts the electrical component by the area it occupies, requiring different length interconnects across an FPGA tile (see section III-A) for different relay technology nodes.

CMOS circuits (in the NEM-CMOS and CMOS-only implementations) are described in a 45 nm technology using the Predictive Technology Model (PTM) suite [29] and a proprietary 45 nm process from STMicroelectronics, with similar results. Global wires are modelled as distributed RC lines, using multiple π sections, based on extracted parasitics for a 5-layer interconnect stack. The primary metrics of interest in the design space exploration are energy, latency and usage of FPGA resources. All of these metrics are specific to the function, while energy consumption and latency are further heavily dependent on data patterns. In order to compare the computational capability of different types of implementations under scaling, different functions including benchmark circuits are synthesised onto the FPGA fabric, and the critical path identified. Circuit-level simulations are carried out (for CMOS, NEM-only and NEM-CMOS implementations) spanning multiple tiles in the FPGA if necessary, and the latency values are calculated as the sum of the stage delays and wire delays in the critical path. The energy consumption of NEM blocks is calculated by adding the mechanical energy and electrical energy components [28] extracted through circuit-level simulations. Details of our modeling and simulation framework is given in a prior paper [30].

For any given combination of relay node and integration node, the tile area of a NEM-only FPGA is estimated based on the number of different types of relays and their footprints. The tile area for a CMOS-only FPGA is estimated based on device count and the ''minimum contactable transistor'' area, i.e. the area occupied by the smallest contactable transistor in the target CMOS process plus the minimum allowed spacing to two sides [31]. For the NEM-CMOS FPGA, the tile area is dictated by the larger of the areas occupied either by the NEM relays or the CMOS that sits underneath.

D. MODEL VALIDATION

1) NEM RELAYS

We have fabricated 3-T and 4-T prototypes (without insulating coupler) corresponding to the largest node in Table 1 for proof of concept of architecture. Figs. 7(a) and 7(b) show micrographs of functioning relays. For a 3-T relay of $L_{eff} = 74$ µm, the pull-in and pull-out voltages are 42 V and 34 V respectively. The deviation of V_{pi} from the FEM simulated value of 49.2 V is within expected variations for the nominal air gap of 1 µm based on limitations in our fabrication process. The measured hysteresis window (difference between pull-in and pull-out) is likely due to surface adhesion forces.

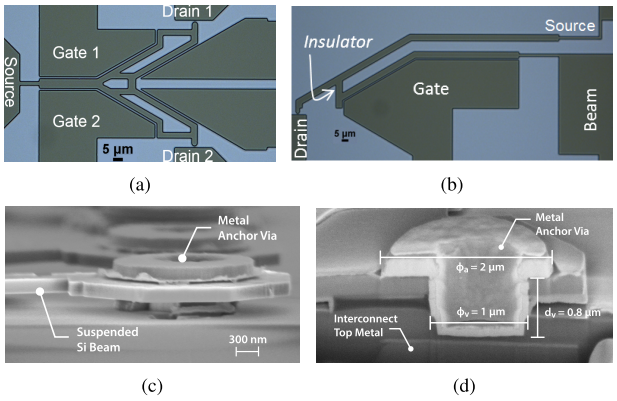


FIGURE 7. Fabricated prototypes: (a) 3-T relay with effective beam length of 74 μm; (b) 4-T relay with effective beam length of 168 μm; (c) integrated silicon NEM relay structure with anchor via (diameter 1 μm) connecting to a metal interconnect stack, and (d) via cross-section.

2) VIA-LAST, HETEROGENEOUS 3-D INTEGRATION

Fabrication experiments have also been carried out to demonstrate proof-of-concept of the adopted heterogeneous integration platform. Shown in Fig. 7(c) is a micrograph of an integrated NEM relay structure. Fig. 7(d) shows the cross-section of the anchoring via connecting the transferred Si device layer to the top metal layer of the CMOS wafer. Resistance measurements of daisy-chained vias have been obtained and this integration node is shown in the scaling roadmap of Fig. 5.

III. NEM RELAY-BASED FPGAs

In this section we describe how CMOS-only, hybrid NEM-CMOS and NEM-only FPGAs are implemented for simulation. The NEM-CMOS FPGA uses CMOS for functional units and NEM relays that stay in their switched state after configuration, in routing switches. In the CMOS implementation, static random-access memory (SRAM) cells are used to store the Look-Up-Table programmable bits as well as the state of the programmable routing switches (NMOS pass transistors). In the NEM and NEM-CMOS implementations NV relays are used for storage.

A. GLOBAL ARCHITECTURE

In this study we use a cluster-based island-style FPGA architecture, predominant in commercial FPGAs [32]–[34], with identical unit tiles arranged in a rectangular grid interspersed with routing channels of width W (see Fig. 8). A unit tile comprises three types of blocks: Configurable Logic Block, Connect Box and Switch Box. The Configurable Logic Block provides reconfigurable logic based on a Look-Up-Table. The Connect Box selectively connects Configurable Logic Block inputs/outputs to designated routing tracks in a channel through configurable routing multiplexers. A Switch Box provides programmable connectivity between horizontal and vertical routing channels, allowing routing tracks to either extend along its current channel or turn a corner to a different channel. Together, the Switch Box and Connect Box form the on-chip programmable interconnect network.

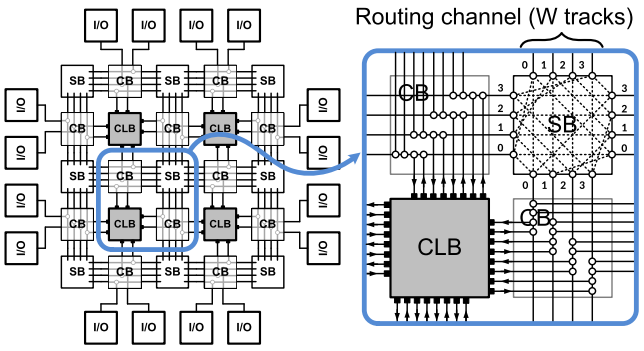


FIGURE 8. Island-style global FPGA architecture. A unit tile consists of Configurable Logic Block (CLB), Connect Box (CB) and Switch Box(SB).

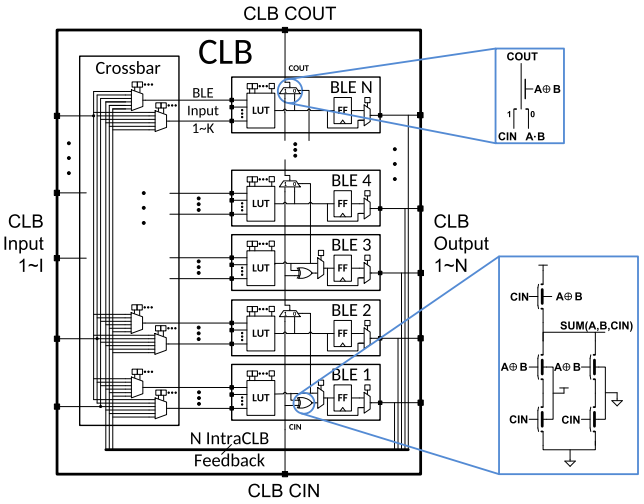


FIGURE 9. Logic architecture of cluster-based Configurable Logic Block (CLB) with I inputs, N outputs, using K-input Look-Up-Table (LUT). NEM relay-based implementation of the dedicated carry-chain (optional) is shown in callouts

B. CONFIGURABLE LOGIC BLOCK (CLB)

A cluster-based Configurable Logic Block of size N contains N Basic Logic Elements (BLE) and has I inputs and N outputs, as shown in Fig. 9. Each Basic Logic Element is a K-input Look-Up-Table whose output can selectively be registered using a D flip-flop. The Look-Up-Table can be configured as any K-input logic function by storing the target function's truth table in programmable memory. Each Basic Logic Element output directly connects to a Configurable Logic Block output pin, and can also feed back to any one of the $K \times N$ Basic Logic Element inputs through a fully-populated multiplexer-based crossbar. The I Configurable Logic Block inputs can also feed any one of the Basic Logic Element inputs through the same crossbar. Our implementation uses the following parameters for a Configurable Logic Block: $K = 4$, $N = 10$ and $I = 22$ (following Ahmed

and Rose's recommendations for Look-Up-Table and cluster size to achieve optimal area-delay trade-off [35]). A dedicated carry-chain is incorporated into the Configurable Logic Block of the NEM-only FPGA (see Fig. 9), which greatly enhances performance of add/sub operations with negligible overall increase in the tile area. Every pair of Basic Logic Elements has a single XOR gate and a 2:1 multiplexer (configured as an AND function). As all 2:1 multiplexer relays along the carry-chain pull in simultaneously, the carry path has only one mechanical delay, in addition to the electrical delay.

C. ROUTING ARCHITECTURE

The channel width W of the global wires that link tiles is a trade-off between routability and tile area. Using the Verilog-to-Routing (VTR) tool set [36], the minimum required channel width W_{min} to successfully route the 20 largest MCNC benchmark circuits[2] [37] is 96 tracks. We choose $W = 160$, similar to a few commercial architectures (eg: [33]) which avoids "high-stress" routing situations, which can severely limit performance, while keeping the number of routing switches to a reasonable number. The links are unidirectional with a single driver scheme [38].

The Switch Box in our designs is based on an architecture proposed by Lemieux *et al.* [38], with a few modifications. The number of tiles that is traversed before being buffered is defined as the routing segment length, L. We adopt a staggered buffering scheme for the different tracks within a channel, so that a fraction $1/L$ of the tracks is buffered at every tile from 1 to L. The Switch Box flexibility, f_s, is defined as the number of output link choices (i.e. one of North, South, East or West) available to each track. Our architecture uses $f_s = 3$, which provides a reasonable compromise between cell complexity and routing flexibility for the NEM-only and NEM-CMOS FPGAs where routing switches are much larger. Finally, in the original architecture, different bit slices of the channel are clustered into routing "domains" where tracks in a certain domain are restricted to connect only to other tracks within the same domain. Our modified architecture allows domain swapping, which greatly increases the routability (see appendix A for details).

An FPGA tile has two Connect Boxes (see Fig. 8) dedicated to input and output links. The fraction of routing wires in a channel that a Configurable Logic Block input or output can connect to is called the connection flexibility f_c [39]. We use $f_{c\_in} = 0.1$ and $f_{c\_out} = 0.25$, meaning an input pin connects to 16 tracks spread evenly across routing domains, and an output pin has access to all routing domains through the two closest Switch Boxes. Implementation details of the Connect Box are given in appendix B.

[2]Widely used set of benchmark circuits developed by the Microelectronics Center of North Carolina (MCNC) for evaluation of floorplanning, placement and routing methods.

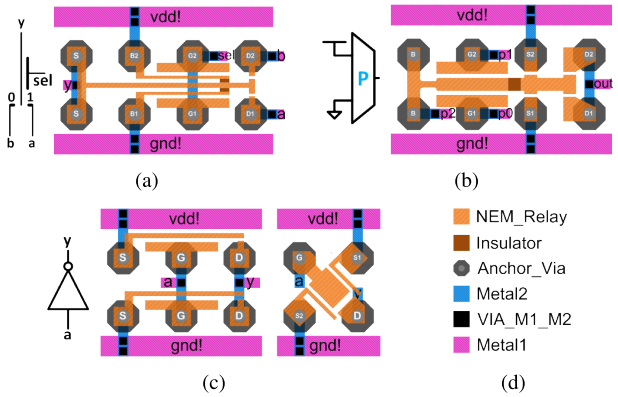


FIGURE 10. Gates constructed from NEM relays: (a) 2-way multiplexer; (b) 1-bit NVM; (c) Inv. with regular (left) and optimised layout (right); (d) Legend.

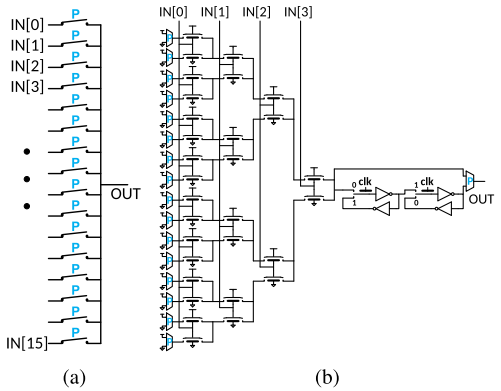


FIGURE 11. Schematic of NEM-based building blocks: (a) 16:1 MUX; (b) BLE.

D. CMOS BUILDING BLOCKS

The main CMOS cells used in the CMOS-only and NEM-CMOS FPGAs are buffers, multiplexers and D flip-flops. The buffer is a tapered inverter chain optimised for the type of load it sees. The D flip-flop is designed using a master-slave arrangement of SR latches built using cross-coupled inverters with active feedback, having minimum-sized NMOS and 2× PMOS FETs. The set-up and hold times in the 45 nm technology are 15 and 0 ps respectively. The 6-T SRAM cells used to store the Look-Up-Table and routing switch configurations in the CMOS-only FPGA are implemented using low-leakage transistors to reduce stand-by power. The routing multiplexer has a double-stage architecture [40] with NMOS pass transistors and a level restorer, with transistor sizes to minimise the area-delay product. This multiplexer architecture offers a reasonable compromise between memory bits and pass transistors.

E. NEM BUILDING BLOCKS

Fig. 10 shows examples of the FPGA building blocks realised from 3-T, 4-T and NV relays. Fig. 10(c) shows an inverter built from two 3-T relays (left), and an optimised layout by combining the gate and drain anchors of the two relays (right) to reduce area. Fig. 10(b) shows a 1-bit non-volatile

memory (NVM) element, while Fig. 10(a) shows a 2-way multiplexer, one of the key building blocks for a D flip-flop, built by combining two 4-T relays. Thus, relays allow circuit-level optimisations in fundamentally different ways from CMOS due to their unique functionality. Given the efficient implementation of memory elements made possible by NV relays, a single-stage routing multiplexer architecture (shown in Fig. 11(a)) offers the highest performance and lowest area. The functional units are built using a combination of NV and standard relays. The Basic Logic Element schematic is shown in Fig. 11(b).

IV. FPGA PERFORMANCE COMPARISON RESULTS

In this section, the results from our study comparing the logic integration density, performance and energy consumption of the three types of FPGAs (NEM-only, NEM-CMOS and CMOS-only) are presented. The two independent scaling parameters, relay node L_{eff}, integration node λ, and on-resistance R_{on} were varied to carry out a thorough design space exploration.

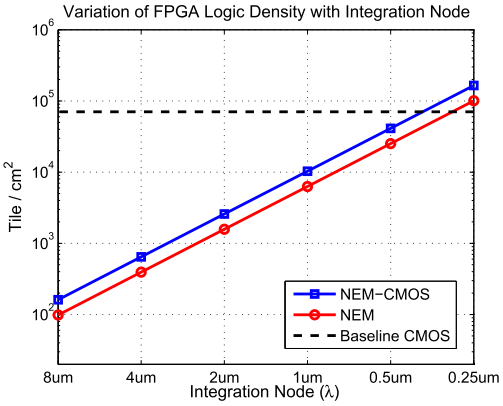


FIGURE 12. Variation of FPGA logic density with integration node.

A. LOGIC DENSITY

The integration rules and NEM device footprints defined in Section III B were used to determine the achievable integration density for NEM-CMOS and NEM only FPGA tiles. Fig. 12 shows the variation of the logic density by scaling the integration node (defined by the via pitch, λ) for the three types of FPGAs. Generally, memory elements constructed from NV relays and routing multiplexers constructed using NV and 4-T relays have far fewer devices than CMOS implementations. The CMOS implementation of the selection multiplexer in particular is quite inefficient compared to the NEM-only version, as it requires a level restorer. However other elements, such as the D flip-flop are more efficient when implemented in CMOS. The NEM-only tile uses fewer devices overall than its CMOS-only counterpart. It matches the area efficiency of the 45 nm CMOS implementation when λ is scaled to 0.3 μm, which is achievable under current technological capabilities (see Fig. 5). The NEM-CMOS FPGA does better than the NEM-only FPGA, as it benefits from

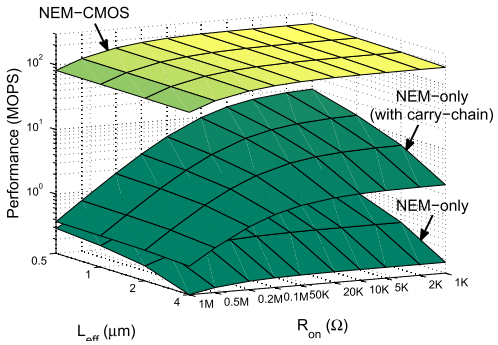


FIGURE 13. Performance of 32-bit ripple-carry adder for 4 NEM relay nodes, when $\lambda = 2$ μm.

the low-device-count NEM implementations of memory and routing multiplexers, and the efficient CMOS implementations of the rest of the circuitry. It breaks even with the CMOS implementation at a via pitch $\lambda \approx 0.4$ μm. For reference, the tile area of the baseline CMOS FPGA is equivalent to 2.5×10^4 minimum contactable NMOS transistors. The tile area of a NEM-only FPGA is equivalent to 3.94×10^3 4-T relays. The tile area of a NEM-CMOS FPGA is dominated by its NEM area at low integration nodes, and equivalent to 3.23×10^3 4-T relays. Its CMOS area is equivalent to 9.99×10^3 minimum contactable transistors.

B. PERFORMANCE

The performance analysis looks at how fast a 32-bit ripple-carry adder and MCNC benchmark circuits [37] can be run, when synthesised on the three FPGA platforms. Simulation of add operations provides insight into the computational efficiency of the NEM-only and NEM-CMOS FPGAs. Fig. 13 shows how adder performance changes under a fixed integration node, $\lambda = 2$ μm, for a range of R_{on} values (R_{on} is much more strongly dependent on contact solutions than relay size). As the integration node is fixed, the area occupied by the adder doesn't change, and wire parasitics remain unchanged. Thus, for the NEM-CMOS implementation that only requires relays to switch during configuration, the result of scaling the NEM relays is to lower capacitive parasitics, whose effect is minimal. For example, for constant R_{on}, scaling L_{eff} from 4 μm to 0.5 μm only provides an improvement of less than 10%, half of which occurs when scaling from 4 μm to 2 μm. Maintaining a low R_{on} on the other hand, is crucial, which may be easier for larger contacts.

In the case of the NEM-only FPGA, as functional units are implemented in NEM relays, the performance is heavily dependent on the mechanical delay, and thus its reduction has a significant effect. When L_{eff} is scaled from 4 μm to 0.5 μm, T_{mec} reduces by a factor 7.3×. Without dedicated carry-chain circuitry in the Basic Logic Element, the performance of the NEM-only FPGA is over two orders of magnitude worse than CMOS-only and NEM-CMOS implementations, as the critical path has multiple relays switching sequentially.

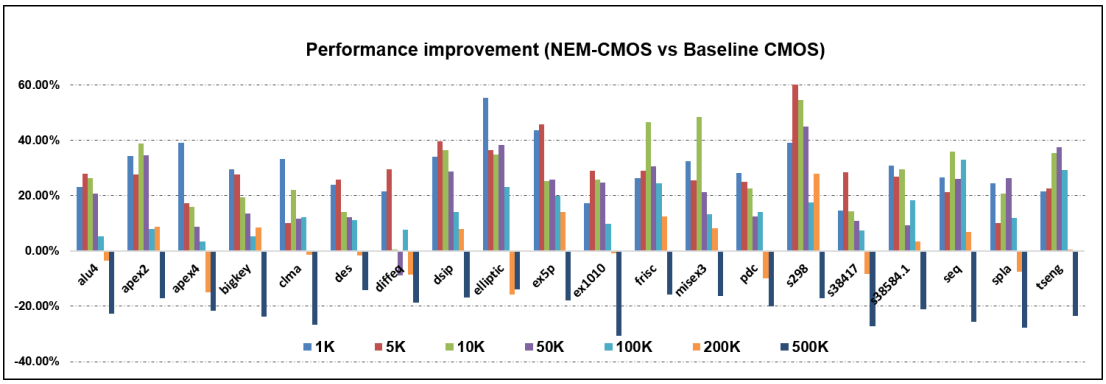


FIGURE 15. Improvement in clock frequency for MCNC20 benchmark circuits placed & routed on the NEM-CMOS FPGA compared to baseline CMOS FPGA.

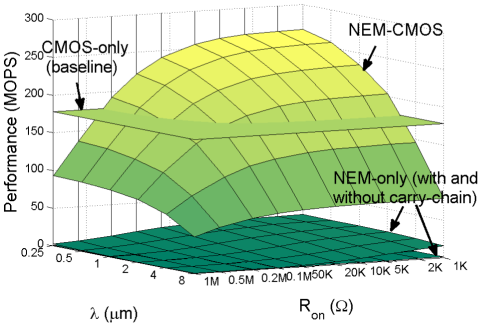


FIGURE 14. Performance of a 32-bit ripple-carry adder, for 6 values of via pitch, with the 0.5 μm NEM relay node.

A dedicated carry-chain results in a 16.4× improvement, with less than 1% increase in area. The overall trend with relay node scaling remains the same with or without a dedicated carry chain.

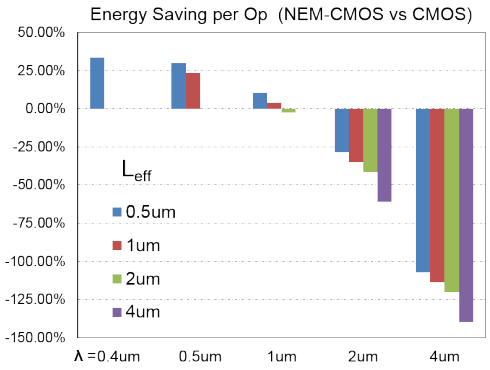
Shown in Fig. 14 is the impact on performance from scaling the integration node, for a fixed relay node of L_{eff} =0.5 μm. Scaling of λ has a significant impact on the overall performance, as it directly affects the area, and thus the length of global wires. When $\lambda \leqslant 0.4\,\mu m$ and $R_{on} \leqslant 200\,k\Omega$, the NEM-CMOS implementation provides an opportunity for higher performance with smaller die area than the baseline CMOS design. For λ =0.4 μm and R_{on} = 1 kΩ, the NEM-CMOS FPGA gives a 1.5× performance improvement over the CMOS-only FPGA for the same area. As the mechanical delay is at least 2 orders of magnitude greater than the electrical delay, the NEM-only implementation has a lower performance, and scaling λ, which has the effect of reducing the electrical delay, has relatively little effect.

Next, we look at how complex designs perform on these FPGA platforms by synthesising the 20 largest MCNC benchmark circuits [37] using the Verilog-to-Routing (VTR) tool set [36]. The netlists resulting from place and route of these circuits are simulated using the parameters and parasitics associated with $\lambda = 0.4\,\mu m$ and $L_{eff} = 0.5\,\mu m$ to extract the critical path latency for a range of R_{on} values. The percentage performance improvement of the NEM-CMOS implementation against the baseline CMOS performance is shown in Fig. 15. Average performance improvements when $R_{on} = 1\,k\Omega, 5\,k\Omega, 10\,k\Omega, 50\,k\Omega, 100\,k\Omega, 200\,k\Omega$ and $500\,k\Omega$ are 30%, 28%, 28%, 21% , 14%, 1%, and -21% respectively. Since VTR routes the target circuits using the minimum number of tracks that can achieve 100% routing, the average performance improvements after place-and-route are smaller than with the manually mapped circuit-level results. R_{on} need only be under 200 kΩ for an overall performance improvement, which is consistent with the previous results.

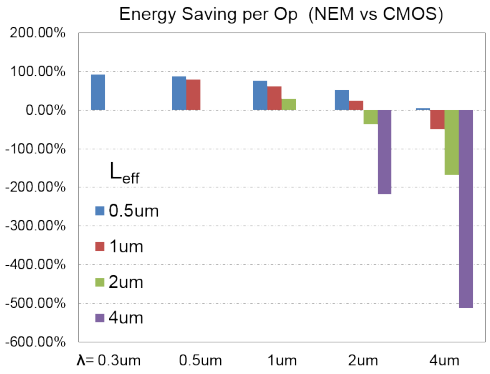
C. ENERGY

Scaled relays can be operated with a smaller V_{DD} and also have a smaller C_{gs}. As can be seen from Table 1, halving the length results in a halving of the gate capacitance, while V_{DD} scales at a slightly slower rate of around 0.75, partly due to the engineered margin with respect to pull-in. As the dynamic energy has the same $CV_{DD}{}^2$ dependence as CMOS, halving the effective length reduces the energy of a single switching transition of a relay by a factor better than $\frac{1}{3}$. An important consequence of the proposed architecture is that the NEM-CMOS FPGA does not have relays switching during normal operation. *Thus the NV relays allow the NEM-CMOS system to be run at the rail voltage required by the CMOS process.* Only the programming phase requires the V_{DD} associated with the relay technology.

Figs. 16(a) and 16(b) show the run-time energy saving for 32-bit addition on NEM-CMOS and NEM-only FPGAs in comparison with the baseline CMOS implementation. The energy consumption is estimated by averaging the energy consumed under a series of random input patterns rather than a single worst-case pattern. The run-time rail voltage for NEM-CMOS is always 1V, while for NEM-only it depends on the relay node as specified in Table 1. Both NEM-CMOS and NEM FPGAs achieve better energy efficiency over the CMOS FPGA when $L_{eff} < 1\,\mu m$ and $\lambda < 1\,\mu m$. For the NEM-CMOS FPGA, the bulk of the savings are from scaling λ, which has a significant effect on the global wire length,



(a)



(b)

FIGURE 16. Energy saving for 32-bit addition against the CMOS baseline for R_{on} =10 kΩ. Only scenarios where the chip area is constrained by λ are considered, i.e. $L_{eff} < N \times \lambda$, where N is the number of device terminals. The NEM-CMOS and NEM-only FPGAs achieve the same area as the baseline CMOS FPGA for $\lambda = 0.4$ μm and $\lambda = 0.3$ μm respectively. (a) NEM-CMOS. (b) NEM only.

and reduces the interconnect dynamic energy. Relay scaling is less important, as the supply voltage remains unchanged at 1 V, and the combined relay parasitic capacitance is much smaller than interconnect capacitance. When $\lambda = 0.4$ μm and $L_{eff} = 0.5$ μm, the NEM-CMOS FPGA has about a 34% energy saving over the CMOS FPGA for the same die area, and can run on a 1.5× faster clock.

For the NEM-only FPGA, device scaling has a significant impact, as the energy consumption is purely dynamic. When $\lambda = 0.3$ μm and $L_{eff} = 0.5$ μm, the NEM-only FPGA with a fast carry-chain has an energy saving greater than 90% compared to the baseline 45 nm CMOS while utilizing the same die area, but is 8.5× slower. At these aggressive integration nodes, the NEM-only FPGA also benefits from not requiring large routing buffers or level restorers, unlike the NEM-CMOS implementation. At larger nodes though, the higher rail voltage and large footprint that results in increased die area and long global interconnects combines to increase the energy consumption above both the CMOS and NEM-CMOS FPGAs.

For the baseline CMOS FPGA, leakage accounts for 17% of the average energy consumption for 32-bit addition during run time. If the mapping leaves a portion of the FPGA unused, the leakage percentage can be much higher, as leakage would generally occur over the entire chip. Fig. 17 shows comaprison of leakage between the NEM-CMOS and CMOS FPGAs. The NEM-CMOS FPGA has a leakage current reduction of 63% and 46% at 27 °C and 85 °C respectively, when the adder is mapped to all the tiles in the FPGA. The NEM-only implementation can achieve near zero leakage in steady state.

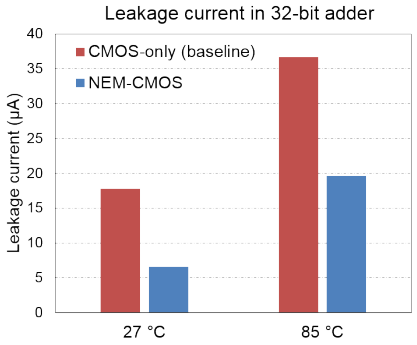


FIGURE 17. Leakage current for 32-bit adder mapped onto baseline CMOS FPGA and NEM-CMOS FPGA, at 27 °C and 85 °C respectively.

V. DISCUSSION AND CONCLUSIONS

NEM relays are known to be inherently radiation-hard and can operate at temperatures > 225 °C with near-zero leakage, while the high mechanical delay does not affect performance when used as routing elements in FPGAs. In this work, we have considered three types of FPGAs, NEM-only, NEM-CMOS and CMOS-only, under a heterogeneous integration scheme and carried out a study to understand how performance, energy consumption, and area compares for various benchmark circuits.

The key to the success of NEM technology is scaling. Technology scaling, however, involves two aspects: scaling of relay dimensions, and scaling of the pitch of the vias connecting NEM relays to the metal interconnect stack. The latter is more of a limiting factor than the device dimensions. Current integration capability does not allow NEM-based chips to achieve an integration density close to that of modern CMOS. However, even with current technological readiness, where the via pitch λ is on the order of a few μm, it is still feasible to fabricate large-scale NEM-based circuits that are at least comparable in performance to nm node CMOS, while providing improvements in energy consumption and harsh-environment capability.

In our study we find that a NEM-CMOS FPGA has superior performance and energy efficiency over a CMOS-only FPGA for the same area where the contact resistance $R_{on} <$ 200 kΩ and via pitch $\lambda \leqslant 0.4$ μm. Given the difficulties with maintaining contact integrity over repeated switching cycles, it is particularly encouraging that a relatively high on-resistance is sufficient to yield performance benefits. The

TABLE 2. Comparison of NEM-CMOS and NEM-only FPGAs with CMOS.

	CMOS	CMOS-NEM	NEM
Performance change	-	up to +50%	−90%
Energy Saving	-	up to +34%	up to +92%
Radiation Hardness	1 Mrad	Unknown	>100 Mrad
Temperature	⩽125°C	⩽125°C	>225°C
leakage change (27 °C)	-	−63%	0 leakage

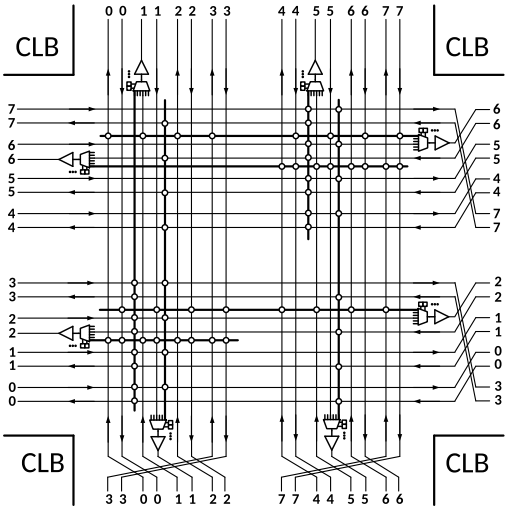


FIGURE 18. Switch Box (SB) architecture with single-driver directional wiring scheme and segment length $L = 4$. A circle represents a cross-over between a routing track and an orthogonal input to a routing multiplexer. Only two routing domains (tracks 0 – 3 and 4 – 7) shown for clarity. Connections between Configurable Logic Blocks (CLB) local to this SB and multiplexers are shown in Fig. 19.

use of NV relays eliminates radiation-induced soft errors associated with bit-flipping common in CMOS SRAM, and the radiation hardness of NEM-CMOS is likely to be considerably higher than a full CMOS implementation, possibly by as much as an order of magnitude. A pure NEM relay-based implementation is not comparable in performance to an advanced CMOS implementation, but is able to operate at temperatures that are limited by soldering and packaging limitations rather than the core junction temperature of a CMOS transistor. Thus, its maximum operating temperature is likely to be closer to 300 °C than the 125 °C to which CMOS implementations are typically rated. Table 2 summarizes the salient properties of each type of implementation in performance, energy consumption and harsh-environment capability. NEM relays with BEOL 3-D integration to CMOS appears to be a promising approach for low power, high performance applications of the future, with enhanced radiation protection. Systems based purely on NEM relays, on the other hand, offer unprecedented harsh-environment capability with zero stand-by power, for lower performance applications.

APPENDICES A
SWITCH BOX (SB) DESIGN

Shown in Fig. 18 is an example of our Switch Box with 16 routing tracks which includes two routing domains, track nos. 0-3 and 4-7. Here, wires are connected at cross-over points only where a circle exists, and the grouped multiplexer inputs are shown by one thick line for clarity; each of the wires connected to this input line are separate inputs to the multiplexer (the track cross-overs that effect changes in track position allow this cross-bar to be replicated and abutted with no modification to realise all of the Switch Boxes [39]). This crossbar unit has 4 buffers and 4 routing multiplexers, and the architecture allows domain swapping for tracks on the South and East ports (for example, track 0 going north can make a right turn into track 6 going east) and track 6 going west can make a turn into track 0 going south). The choice of $L = 4$ restricts the percentage of tracks that can turn to 25% (i.e. $1/L$) at a maximum. The domain swapping, however, appears to increase the flexibility to the point that $L = 4$ is almost as routable as $L = 1$ (when tested for place and route of benchmark circuits using the Verilog-to-Routing (VTR) tool [36]), while greatly reducing cell complexity.

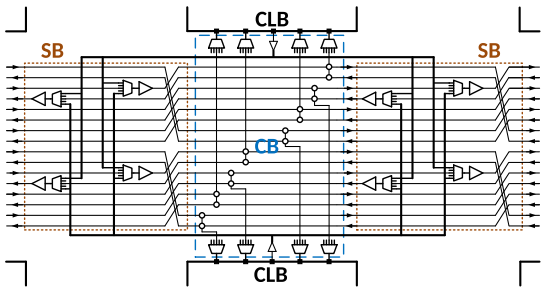


FIGURE 19. Connect Box (CB) architecture. The output CB is incorporated into the Switch Box (SB). A circle represents a connection between a routing track and Configurable Logic Block (CLB) input multiplexer. Only one CLB output and four CLB inputs are shown for clarity.

APPENDICES B
CONNNECT BOX (CB)

The Connect Box (architecture shown in Fig. 19) provides connectivity to and from an Switch Box to its associated Configurable Logic Block, with two Connect Boxes per tile, dedicated to input and output links. The output Connect Box is incorporated into the Switch Box using a single-driver directional wiring scheme. As all tracks are directly driven by directional buffers, a Configurable Logic Block output connects to a wire through a routing multiplexer in its vicinity.

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